AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 2, lines 4-19 with the following amended paragraph:

A1

Typically, the maximum speed of the memory address/data bus decreases as the number of memory components increases. This ~~increase~~ decrease is caused by, among other things, an increase in propagation delay because of additional capacitive loading. Memory controllers are generally set to output a memory clock having a speed compatible with the maximum number of memory components that can be coupled to the microprocessor. In some applications, the speed of the memory components may change dynamically, thereby creating the need for a memory controller to change the speed of its operating address/data bus dynamically. Therefore, operating the memory controller at a speed compatible with the actual number and characteristics of memory components, such as speed, may be advantageous. Often, this is not being done.